

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A system, comprising:
2 a processor that executes an algorithm;
3 a hardware unit that comprises one or more physical resources;
4 and
5 an abstraction layer implemented by said processor that
6 facilitates communication between the algorithm and the
7 hardware unit through the use of a plurality of functions
8 and that creates a reference to a logical resource that
9 is associated with a corresponding physical resource, the
10 plurality of functions comprise command functions that
11 request and grant ~~the~~ an identifier to the algorithm
12 including a command function that branches to a function
13 that is optimized for ~~the~~ configured settings of the
14 logical resource based upon ~~the~~ a vector table that
15 associates the reference to a logical resource with a
16 memory location of the function that is optimized, and
17 wherein each logical resource is associated with at least one
18 private state that represents ~~the~~ most recently
19 configured settings of the logical resource.

1 2. (Original) The system of claim 1 wherein the reference
2 comprises a pointer to the logical resource.

1 3. (Original) The system of claim 1 wherein the plurality of
2 functions are selected from the group consisting of command
3 functions that request and grant the identifier to the algorithm,
4 configuration functions that pre-compute and store register values
5 and algorithm settings, synchronization functions that align the

6 logical resource with the physical resource, and a combination
7 thereof.

4. (Canceled)

1 5. (Previously Presented) The system of claim 1 wherein the
2 command functions comprise a function that monitors the physical
3 resources and updates a corresponding vector table that associates
4 the reference to a logical resource with a memory location of
5 function optimized for a current operation.

1 6. (Previously Presented) The system of claim 1 wherein the
2 command functions comprise a function that does not write to a
3 register associated with the physical resource if a previous use of
4 the physical resource has left the register in a state compatible
5 with a current operation.

7. (Canceled)

1 8. (Previously Presented) The system of claim 1 wherein the
2 function that branches and the function that is optimized for the
3 configured settings comprise functions with identical function
4 signatures.

9. (Canceled)

1 10. (Currently Amended) A system, comprising:
2 a processor that executes an algorithm;
3 a hardware unit that comprises one or more physical resources;
4 an abstraction layer implemented by said processor that
5 facilitates communication between the algorithm and the
6 hardware unit through the use of a plurality of functions

7 and that creates a reference to a logical resource that
8 is associated with a corresponding physical resource,
9 wherein the plurality of functions are selected from the
10 group ~~comprise~~ comprising configuration functions that
11 pre-compute and store register values and system state
12 settings, and wherein the configuration functions
13 comprise a function that selects and stores an address of
14 a function that is optimized for a current operation; and
15 wherein each logical resource is associated with at least one
16 private state that represents ~~the~~ most recently
17 configured settings of the logical resource.

1 11. (Currently Amended) A method for achieving ~~high-performance~~
2 hardware abstraction, comprising:

3 creating a reference to a logical resource that is associated
4 with a corresponding physical resource;
5 associating with the logical resource one or more private
6 states that represents ~~the~~ most recently configured
7 settings of the logical resource; and
8 executing a plurality of functions that facilitate
9 communication between the physical resource and an
10 algorithm, wherein the plurality of functions comprise
11 command functions that request and grant ~~the~~ an
12 identifier to the algorithm including a function that
13 branches to a function that is optimized for the
14 configured settings based upon ~~the~~ a vector table that
15 associates the reference to a logical resource with a
16 memory location of the function that is optimized.

1 12. (Original) The method of claim 11 wherein the reference
2 comprises a pointer to the logical resource.

1 13. (Original) The method of claim 11 wherein the plurality of
2 functions are selected from the group consisting of command
3 functions that request and grant ~~the~~ an identifier to the
4 algorithm, configuration functions that pre-compute and store
5 register values and algorithm settings, synchronization functions
6 that align the logical resource with the physical resource, and a
7 combination thereof.

14. (Canceled)

1 15. (Previously Presented) The method of claim 11 wherein the
2 command functions comprise a function that monitors the physical
3 resources and updates a corresponding vector table that associates
4 the reference to a logical resource with a memory location of
5 function optimized for a current operation.

1 16. (Previously Presented) The method of claim 11 wherein the
2 command functions comprise a function that does not write to a
3 register associated with the physical resource if a previous use of
4 the physical resource has left the register in a state compatible
5 with a current operation.

17. (Canceled)

1 18. (Previously Presented) The method of claim 11 wherein the
2 function that branches and the function that is optimized for the
3 configured settings comprise functions with identical function
4 signatures.

19. (Canceled)

1 20. (Currently Amended) A method for achieving ~~high-performance~~
2 hardware abstraction, comprising:

3 creating a reference to a logical resource that is associated
4 with a corresponding physical resource;

5 associating with the logical resource one or more private
6 states that represents ~~the~~ most recently configured
7 settings of the logical resource; and

8 executing a plurality of functions that facilitate
9 communication between the physical resource and an
10 algorithm, wherein the plurality of functions comprises
11 configuration functions that pre-compute and store
12 register values and algorithm settings and wherein the
13 configuration functions comprise a function that selects
14 and stores an address of a function that is optimized for
15 a current operation.

21 to 30. (Canceled)